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1 6.) The method according to claim 5, wherein the step of applying telephone line
2 power further includes the step of applying line power when the detected voltage
3 exceeds the absolute value of one P-channel threshold voltage plus one N-channel
4 threshold voltage in the electronic circuit.

1 7.) The method according to claim 1, further comprising the step of applying a reset
2 signal to the electronic circuit.

1 8.) The method according to claim 7, further comprising the step of turning-off the
2 reset signal to the electronic circuit after the step of applying telephone line power
3 to the electronic circuit.

1 9.) The method according to claim 1, further comprising the step of entering an active
2 state in the electronic circuit when the telephone line activates, after the step of
3 applying line power to the electronic circuit.

1 10.) The method according to claim 1, further comprising the step of storing up charge
2 from the telephone line prior to the step of applying telephone line power to the
3 electronic circuit.

1 11.) The method according to claim 10, further comprising the step of dissipating the
2 stored up charge across the electronic circuit when the detected voltage exceeds a
3 selected voltage level.

12.) A method of powering a data access arrangement with a telephone line, the data access arrangement having a CMOS electronic circuit, the method comprising:

applying a reset signal to the data access arrangement,

detecting the voltage across the telephone line while the telephone line is in an on-hook state,

powering the data access arrangement with telephone line power when the detected voltage exceeds a voltage necessary to properly operate the CMOS electronic device, and

turning-off the reset signal to the electronic circuit after powering the data access arrangement.

13.) An apparatus for powering an electronic circuit with telephone line power, the apparatus comprising:

a voltage detector that measures the voltage across the telephone line and that generates a Reset signal based on a characteristic of the measured voltage, and

a switch, operably coupled with the voltage detector, for applying telephone line power to the electronic circuit in response to the generated Reset signal.

14.) The apparatus according to claim 13, wherein the voltage detector includes circuitry for generating the Reset signal when the measured voltage exceeds a selected voltage.

1 15.) The apparatus according to claim 13, wherein the voltage detector further includes
2 circuitry for limiting the dc current drain from the telephone line through the
3 voltage detector to < 1.0 microamps.

1 16.) The apparatus according to claim 13, wherein the apparatus further includes a
2 signal path for operably coupling the Reset signal from the voltage detector to the
3 electronic circuit.

1 17.) The apparatus according to claim 14, wherein the voltage detector further includes
2 circuitry for resetting the electronic circuit until the measured voltage exceeds the
3 voltage necessary to properly operate digital logic in the electronic circuit.

1 18.) The apparatus according to claim 17, wherein the voltage detector further includes
2 circuitry for enabling the electronic circuit after the measured voltage exceeds the
3 absolute value of one P-channel threshold voltage plus one N-channel threshold
4 voltage in the electronic circuit.

1 19.) The apparatus according to claim 13, further comprising a electronic charge
2 storage device operably coupled to the switch, such that the storage device
3 accumulates electronic charge when the telephone line power is disconnected
4 from the electronic circuit and such that the storage device provides electronic
5 charge when the telephone line power is applied to the electronic circuit.

- 1 20.) The apparatus according to claim 13, further comprising a high impedance
2 resistor connected in series with the electronic circuit for limiting the voltage
3 applied across the electronic circuit.
- 1 21.) The apparatus according to claim 16, further including a time delay element
2 coupled along the signal path between the voltage detector and the electronic
3 circuit, such that the delay element delays application of the Reset signal at the
4 electronic circuit.

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